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DEVELOPMENT OF CHARGE TRANSFER DEVICES FOR 1-2 MICRON IMAGING.(U)
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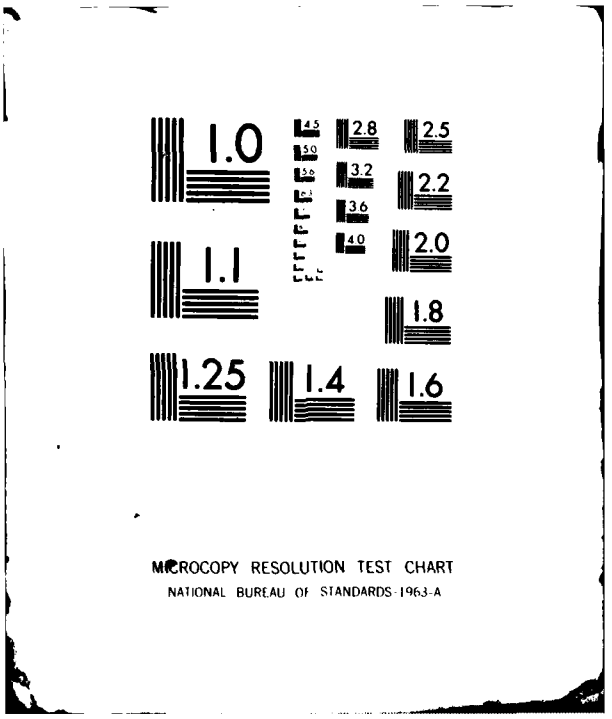
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1.0 INTRODUCTION

There are a number of military applications for a passive (available illumination) night vision capability. Technological advances in image intensifiers and high performance photocathodes have resulted in night vision systems which operate in the visible and near infrared spectrum under low level moonlight and starlight illumination. These systems are, however, completely ineffective under moonless or overcast conditions because of the low level of light in the 0.5-0.9μm region under such conditions. Since there is considerable night glow ambient illumination in the 1.0-1.8μm wavelength region which is nearly independent of cloud cover, one solution to this problem is the development of an imaging system which operates in this wavelength region.

The development of a 1.0-1.8μm imaging system has been the goal of a number of research efforts over the past 10 years. Most of these efforts have been directed at the development of a photocathode which would work in the 1.0-1.8μm region. In spite of the large number of device concepts examined, none has yet emerged as a viable candidate to meet the requirements for a 1.8μm imaging photocathode. A potential alternative to a photocathode for infrared imaging is the charge coupled device (CCD). While Si CCD's have recently coome to the forefront for both visible and 3-5μm imaging applications, there are no suitable deep level impurities in this material for operation in the 1-2μm region. Furthermore, Si devices designed for 3-5μm, require cooling to ~40K for satisfactory operation. Such cooling requirements would make Army night vision devices prohibitively expensive and would place unacceptable restrictions on virtually all of the 1-2μm imaging systems envisioned for Army applications. CCD's developed in new materials with high optical absorptaion coefficients in the 1-2μm region offer a viable solution to the systems requirements for a 1-2μm imaging system.

The approach that we are pursuing in this program is the development of a non-MIS heterojunction CCD. This approach is chosen because of the present lack of a viable MIS technology for materials other than silicon and recent developments at the Science Center on non-MIS devices. In spite of the

extensive studies of III-V MIS devices, significant problems still remain to be solved in order to fabricate a useful III-V MIS CCD. While significant progress has been made in reducing the surface state density on some MIS structures, the mobile ion and insulator stability problems in low temperature deposited or anodic insulators have remained. These problems prevent the realization of a MIS CCD with stable and reproducible characteristics.

There is now reason to believe that a buried channel heterojunction may not only avoid the above problems associated with insulators in a MIS CCD, but offer certain inherent advantages which render it more suitable for the 1.8μm imaging application. Some of these advantages are:

(1) A built-in anti-blooming capability without the use of special channel stop regions.
(2) Superior radiation hardness to both particle (electrons, protons) and photon (x-rays, gamma rays) irradiation.
(3) Greater dynamic range because of low charge generation and absence of an insulator.
(4) High optical quantum efficiency achieved with intrinsic direct bandgap III-V materials.
(5) Lower dark current because the electric field is confined to a wide bandgap charge transport layer in a heterojunction device.

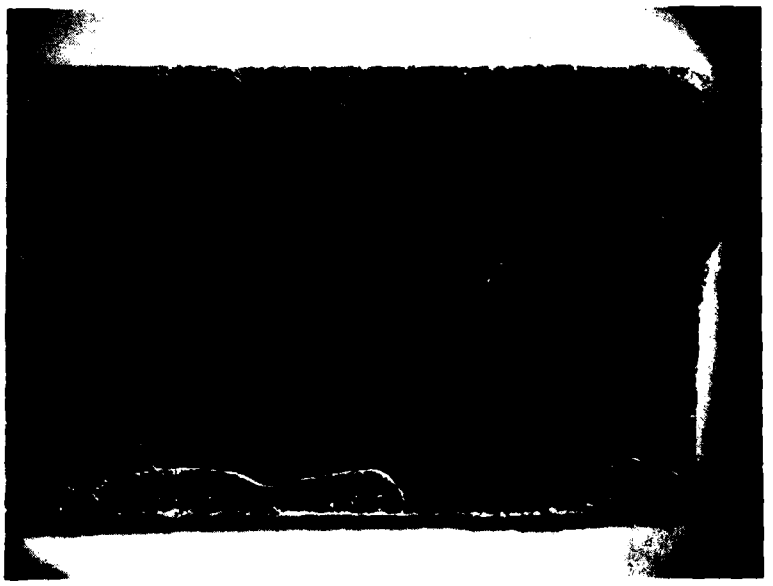
Thus, heterojunction CCDs promise a very exciting approach to 1-2μm imaging. While several material systems are potentail candidates for this application, the GaAlSb-GaSb system is selected for the first development phase because it offers the potential to demonstrate a heterojunction CCD with a relatively simple Schottky barrier structure. We also have extensive experience in device applications of this material system. With this material system, at the expected average signal levels in this application, photon shot noise limited operation should be realizable.

2.0 PROGRESS

During this reporting period, several important accomplishments can be reported. Most significantly, the first heterojunction CCD was successfully operated. This device consisted of four gates, and is entirely planar. This demonstration was made possible because of the drastically improved epilayer surface morphology made possible by addition of As to the melt which results in a quaternary structure active layer, GaAlAsSb. Figure 1 shows the surface of one such wafer. One of the devices fabricated from the new quaternary wafers is shown in Fig. 2. The selection of devices suitable for bonding proceeds as follows: All the devices which do not have obvious lithographic flaws are probed one at a time. First, the device is tested for shorts between gates and shorts to the guard ring. Next the guard ring is tested for leakage. Finally, the ohmic contacts are tested by measuring the I-V characteristic between the input and output ohmic contacts. Unfortunately, this test is not conclusive at this stage, since the I-V characteristic does not distinguish between ohmic contacts that are properly formed and those which are shorted to the substrate. Measuring the I-V characteristic between an ohmic contact to the n-layer and the bottom substrate contact is also not conclusive. Normally, this test should result in a normal p-n diode characteristic, where the reverse bias condition corresponds to the reverse bias of the p-n junction. In this case, since the areas of the p-n junction is uncontrolled, a large leakage current is measured which is often indistinguishable from a shorted p-n junction. The solution to this problem is, of course, a guarded diode consisting of an ohmic contact dot surrounded by a Schottky guard ring which can be biased to isolate the p-n junction, in much the same way it is done in the CCD channel-stop.

Devices which exhibit no shorts and which have good ohmic contacts can be bonded up as CCDs. Even if ohmic contacts have not been formed, the device is useful for charge storage experiments. In fact, several devices like this have been bonded up and tested.

(a)



(b)

Fig. 1 Comparison of early GaAlSb epi-layer (a) with new GaAlAsSb layer (b). Wafer (b) is 1cm x 2cm.

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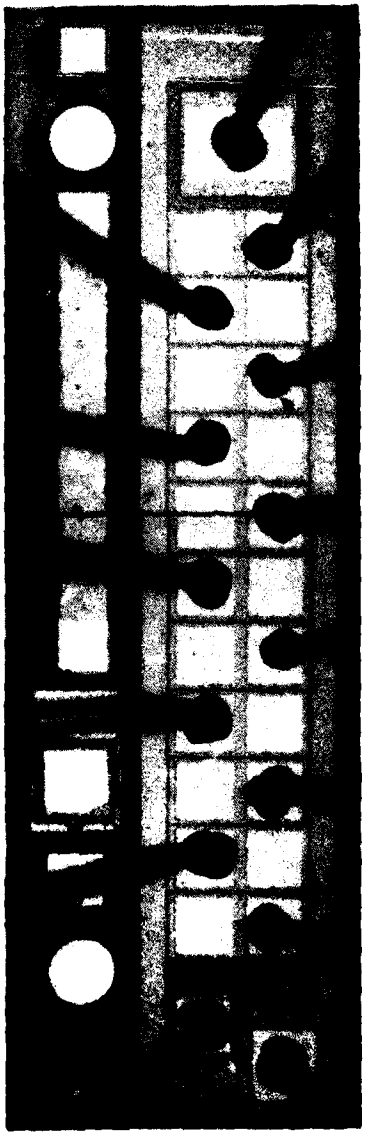

Fig. 2 GaAlAsSb/GaSb CCD structure.

The first experiment performed with one of these devices (K103) was to verify the charge storage effect in this planar structure. This experiment is important because it verifies the concept of using a biased guard ring for a channel stop. For this experiment, the guard ring is biased with a negative voltage sufficient to deplete the active layer and therefore isolate the device active area from the rest of the wafer. In this way, the isolation between a signal charge pocket and the rest of the wafer is the same as the isolation between transfer gates.

To perform this experiment, capacitance as a function of time is measured after the active region has been depleted of carriers. All the tansfer gates are tied together and form one terminal of the test capacitor. the substrate is the other terminal. The guard ring is connected to an adjustable negative power supply. The measurement is initialized by pulsing the gates so that they are depleted. The capacitance is then measured as a function of time to determine how long it takes for equilibrium to be re-established. This is the charge storage time. The best charge storage time measured was 800 sec at 77°K. This experiment is, of course, carried out in the dark. If the sample is illuminated during the experiment, the capacitance rapidly returns to the equilibrium value. The total gate area in this device was $4.3 \times 10^{-3} cm^2$. Much longer storage time should be attainable in the future. One problem with this initial experiment was that the potential outside of the guard ring was not controlled. This potential can float arbitrarily and can lead to dark current contributions from the rest of the wafer. In future experiments, this potential will be "pinned" to a value somewhat more positive than the guard ring potential to prevent electrons from the epilayer outside the device from contributing to dark current.

The most important test is to operate a device as a CCD and observe charge transfer. Such a test was successfully performed on Oct. 11, 1978. The major problem experienced in the attempt to perform this test was the lack of good ohmic contacts. In fact, in the first demonstration of charge transfer in the heterojunction CCD, the device selected had only one usable ohmic contact. A defect had, however, caused the Schottky barrier of gate

number 6 to be leaky. This gate was used as the output ohmic contact. From then on, the configuration was quite conventional.

Figure 3 shows the configuration of the first charge transfer demonstration. The input and output (Gate 6) ohmic contacts are biased to a positive voltage and are capacitatively coupled for signal input and output. The input pulse is synchronized to occur when ϕ_2 is positive. Therefore, the first clocked gate must be ϕ_2. The last gate is grounded so that it acts as a barrier for the charge pocket (see Fig. 3, T4 and T5). the remaining gates are tied to ϕ_3 and ϕ_1. The output pulse can be seen to occur when ϕ_1 makes a positive to negative transition. Figure 4 shows the results of this experiment. Figure 4a shows the input and the time delayed output pulse. Figure 4b shows the relation of these pulses to the clock phases. As can be seen from a study of Fig. 3, this experimental arrangement results in charge being injected into the first clocked gate (ϕ_2) every cycle.

This is the reason for the small difference between the output signal level and the background. Although this device consisted of only four gates, it is an encouraging first step and is a precursor to a larger device being operational, now that improved material technology has been achieved.

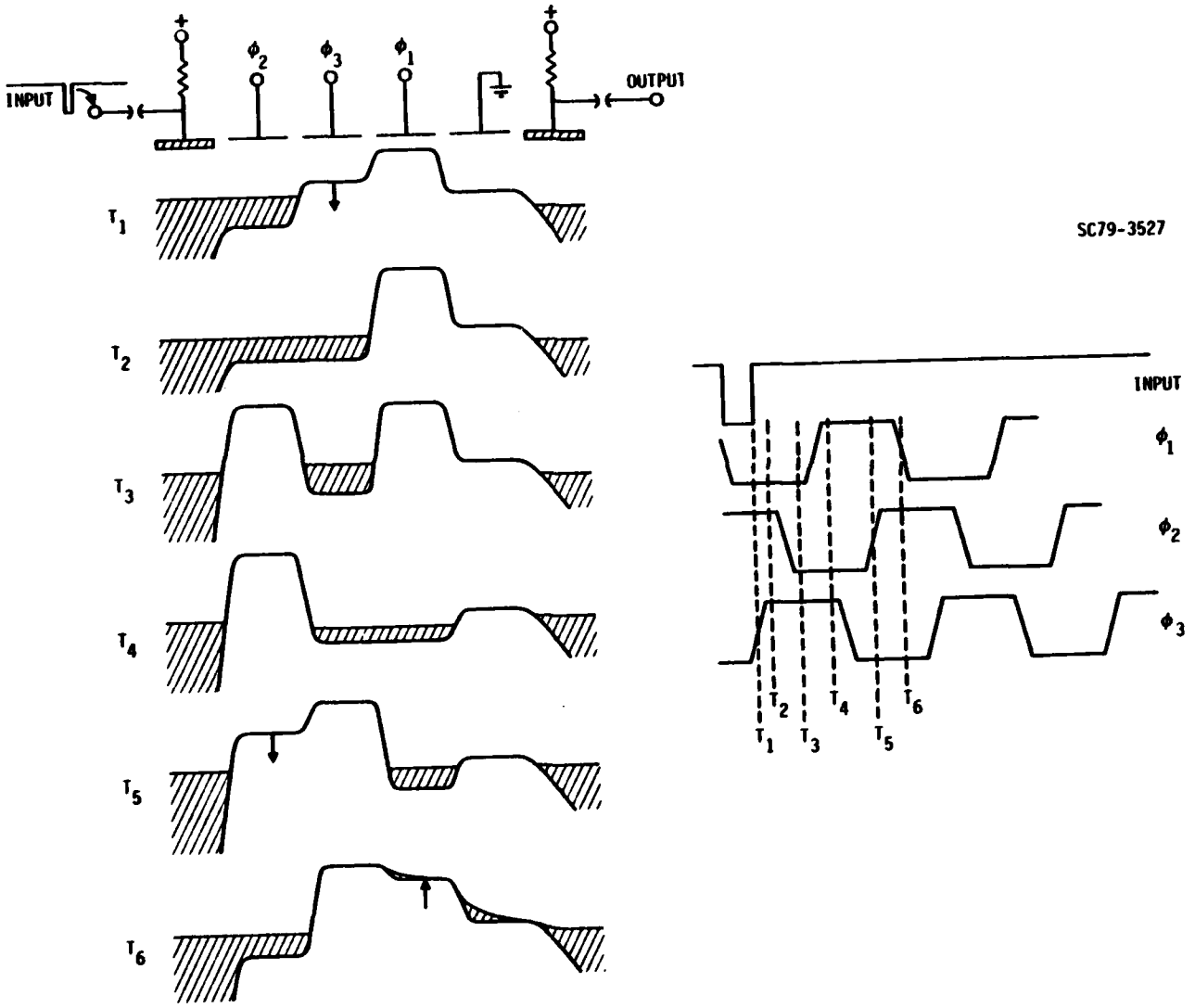

Fig. 3 Heterojunction CCD experimental set-up and timing diagram.

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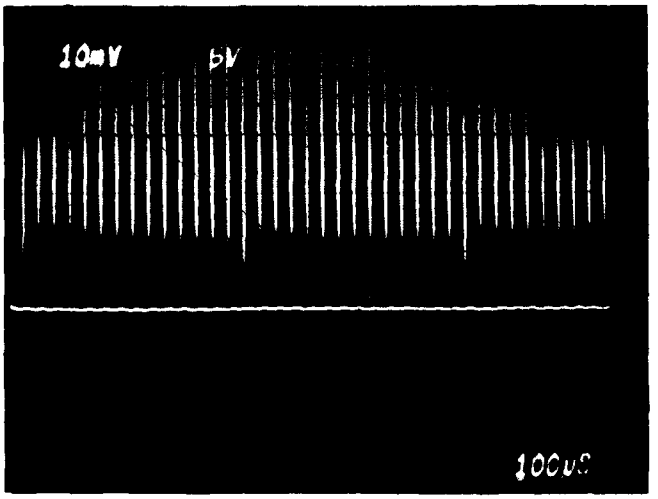
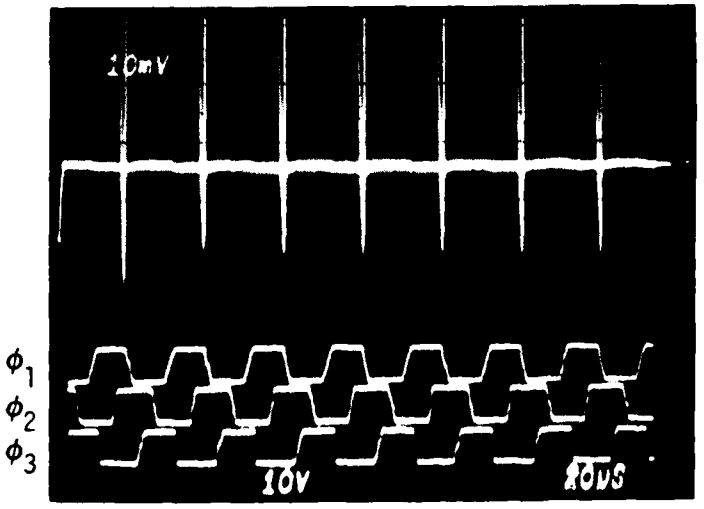


(a)



(b)

Fig. 4 (a) HJCCD output (top) and input pulse (bottom); (b) HJCCD input and output (top two waveforms) and 3 phase clocks, (bottom).

3.0 CONCLUSION AND RECOMMENDATIONS

This report marks the end of the current phase of the program to develop a charge coupled image sensor for the 1-2μm spectral region. At this point, it is appropriate to summarize the results, discuss the difficulties, and project future progress toward the ultimate goal of a large area (400 x 400 pixels) image sensor.

The most important results are, as discussed in Section 2, the vastly improved GaAlAsSb material quality, in particular the improved surface quality. The material quality at present is such that 1mm x 1mm focal planes can be fabricated with usable yield. The second significant result is that it was demonstrated that the guard ring isolated device is feasible. Using a guard ring isolated device scheme, a focal plane can be designed which requires only 4 masking steps (including 2 level metalization), of which only 1 has critical tolerances and small (~1μm) line widths. Finally, a prototype CCD in the GaAlAsSb/GaSb heterostructure was successfully operated. This is the first demonstration of CCD operation in a heterojunction structure. It is a significant first step since it opens the way for what is potentially a very high performance CCD imager technology.

Also significant, a wafer of GaAlSb/GaSb supplied by the Science Center was successfully fused to Corning 7056 glass by Dr. John Pollard at Night Vision Labs. This is a crucial part of the final imager design.

The only significant difficulty remaining is the formation of ohmic contacts to the n-GaAlAsSb epitaxial layer. Most of the difficulty arises from the native oxide which is invariably present on the epilayer surface. This problem can be alleviated most satisfactorily by growing a thin (~1000A) layer of n^+ GaSb on top of the n-GaAlAsSb. Subsequent etching of the n^+ GaSb from the surface everywhere except where ohmic contacts are desired, will substantially enhance formation of ohmic contacts. Alternatively, the GaAlAsSb surface can be covered with evaporated or sputtered oxide, then etched in a solvent which attacks the native oxide. Immediate evaporation of ohmic contact metalization will result in uniform subsequent alloying.

Yet a third method, which will be possible with the installation of a new piece of process equipment, is to sputter etch the surface where the ohmic contact is desired and perform an in situ metalization. The GaAlAsSb/GaSb technology is now at the stage where the next logical major step is the development of a device with considerably greater gate complexity than the existing initial device. For example, devices with approximately 100 gate complexity can be fabricated. Such a device would, if arranged as a linear array, permit the evaluation of transfer efficiency, characterization of bulk traps, and dark current. An imager can also be fabricated to allow evaluation of spectral response and sensitivity. From that point on, the development of larger area imagers will be paced, essentially by continued material development. This is partly due to the fact that Schottky gate integrated fabrication techniques are rapidly being developed at the Science Center in other programs and, therefore, problems such as multi-level metalization are not expected to hamper progress.

FIGURE CAPTIONS

Fig. 1 Comparison of early GaAlSb epilayer (a) with new GaAlAsSb layer (b). Wafer (b) is 1cm x 2cm.

Fig. 2 GaAlAsSb/GaSb CCD structure.

Fig. 3 Heterojunction CCD experimental setup timing diagram.

Fig. 4a HJCCD output (top) and input pulse (bottom).

Fig. 4b HJCCD input and output (two two waveforms) and 3 phase clocks (bottom).